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TEM/SEM INVESTIGATION AND ELECTRICAL EVALUATION OF A BOTTOMLESS I-PVD Ta(N) BARRIER IN DUAL DAMASCENE

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ABSTRACT

A barrier deposition technique, named as 'bottomless I-PVD Ta(N)', has been developed and evaluated on copper dual damascene. A re-sputter step was added to a standard barrier deposition recipe. In the re-sputter step the previously deposited barrier is removed from the via bottom. As a result of the physical sputtering, the barrier deposited onto the metal 2 trench bottom is thinned. However, due to the non-conformal deposition of the I-PVD, a process window exists, hence it is possible to remove the barrier from the via bottom and still maintain some barrier on the metal 2 trench bottom. As a result of the removal of the barrier layer from the bottom of the via, the contact resistance is decreased as compared to standard deposition recipes.

INTRODUCTION

Copper interconnects processed with a dual damascene approach have a barrier layer at the via bottom. The presence of the barrier layer at the bottom of the via can cause an increase in via resistance. Furthermore, the barrier metal at the bottom hinders the flow of copper atoms during current stressing. Discontinuity in the copper flux results in void formation and poor electromigration (EM) performance. A schematic representation of a typical EM failure is given after current stressing in figure 1a,b [1]. At the cathode end of the line voids are formed due to material depletion, while at the anode end hillocks or extrusions are expected due to material accumulation [2-4]. If the barrier layer was not present on the via bottom, then better EM-performance is expected, since one of the flux divergent points is removed from the interconnect (Figure 1c). Furthermore, due to the elimination of the high resistivity barrier layer a decrease in via resistance is expected. By having copper on copper contact at the metal 1/via interface one can also expect a better electroplating performance during processing.

The present contribution deals with the development of an I-PVD Ta(N) barrier deposition recipe that removes the barrier layer from the via holes.

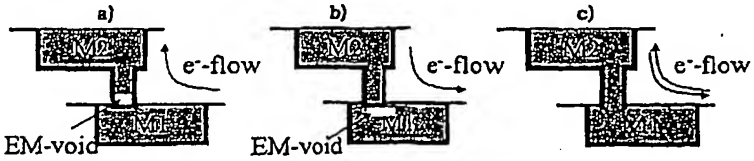

Figure 1 Schematic representation of a dual damascene copper architecture.
a,b) EM induced void formation with a standard barrier on metal 2 (M2)/via level
c) bottomless barrier on M2/via level: no EM-voiding

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EXPERIMENT

A new PVD sequence to remove the barrier metal from the bottom of the vias in a standard ion metal plasma sputtering system named as "Bottomless I-PVD" was developed on an AMAT Electra I-PVD Ta-chamber for 8 inch wafers. A step, in which the barrier metal deposited onto the wafers is re-sputtered, was added in the sputtering sequence in the same chamber as for the precedent deposition of the I-PVD barrier layer. A similar concept with a different purpose (sidewall coverage improvement of PVD tungsten) has recently been discussed in [5]. In the re-sputter step the barrier metal is removed from the bottom and redistributed onto the sidewall of the via holes. During this step the nitrogen flow is removed from the chamber in order to avoid target poisoning.

For electrical evaluation a dual damascene architecture was used. On metal 1 level 500 nm SiO_2 was taken as dielectric with 50 nm SiC and 200 nm SiON ARC capping layer. In patterning the DUV lithography target was on 0.25 µm. For trench filling I-PVD Ta(N)+Cu-seed with ECD copper was used. The excess metal was removed by a two step CMP process. On via and metal 2 levels Flare™ was taken as dielectric with SiC intermediate and SiO_2 as top hard masks. In the DUV lithography the 0.25 µm node was targeted. The dual damascene etch was realized by a "via first at via level" approach. Then I-PVD Ta(N) layer followed by I-PVD Cu seed was deposited. The trench/via holes were filled with electroplated copper and the excess metal was removed by a two-step CMP. For passivation 50 nm SiC with 500 nm Si_3N_4 was taken as dielectric and on the copper bonding pads 30 nm Ta(N) and 300 nm Al were deposited. The excess Al and Ta(N) were removed by CMP.

RESULTS

Simulation of re-sputtering

The application of a barrier that covers the dual damascene recess except the bottom of the via requires a close control of the deposition process. To aid the understanding of the mechanism of the sputter process SIMBAD simulations [6] were carried out. Ionised-PVD provides some selectivity of deposition by ionising a fraction of the sputter flux as the barrier atoms traverse a plasma. The ionised fraction is subsequently aligned to the normal of the surface by the potential difference between the plasma and the wafer [7]. Fig. 2a shows the simulated coverage of a trench by a barrier metal if half of the sputter flux is ionised. The details of the simulation are described in reference [8]. The layer is much thicker at the bottom than at the sidewall. Furthermore the bottom and the sidewall coverages are non-uniform. The layer at the bottom is dome shaped whereas the sidewall coverage decreases with increasing depth. This process is obviously not suited for the deposition of a bottomless barrier.

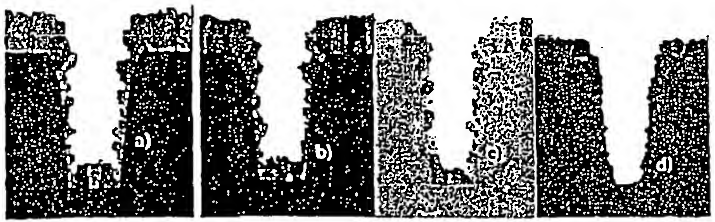

Figure 2 SIMBAD simulation of the profile of a barrier layer over a trench recess. (a) Layer deposited by ionised PVD. 50% of the metal ions are ionised and therefore, aligned to the surface normal. (b) Re-sputtering of the barrier by Argon ions. Metal flux : Argon flux = 9:1. (c) Metal flux : Argon flux = 1:1. (d) Metal flux : Argon flux = 1:9.

The profile of the barrier can, however, be adjusted by adding another component, i.e. Argon ions, that re-sputters simultaneously the barrier layer as it is deposited. Fig. 2b displays a cross-section of a layer, which had undergone Argon bombardment. The ratio of the Argon flux over the barrier metal flux was 1:9. The thickness of the layer on the field has not changed noticeably. This is presumably due to the re-deposition of the re-sputtered barrier atoms. At the bottom of the recess the layer is more uniformly distributed. When the Argon flux is increased to a ratio of 1:1 the re-sputtering of the barrier layer inside the feature becomes more pronounced. The sidewall coverage increases in the lower half of the recess whereas the bottom coverage decreases. The re-sputtering of the barrier metal is related to the angular dependence of the sputter yield. In this simulation the sputter yield peaks at an angle of around 45° and then decreases rapidly for more oblique angle bombardment. Since the Argon ions have an angle of incidence, which is normal to the surface, the barrier is efficiently removed at the bottom of the recess. The re-sputtered atoms from poly crystalline targets are generally ejected from the surface under a pattern, which can be described by a cosine distribution [9]. A large portion of the re-sputtered atoms will be re-deposited at the sidewall of the recess. There, however, the sputter process is very inefficient due to the angular dependence of the sputter yield. Consequently the bottom coverage decreases in a recess whereas the sidewall coverage improves as the bombardment is increased. A further increase of the Argon flux to a ratio of 9:1 gives rise to a thinning of the barrier not only at the bottom of the recess, but also on the field. It also produces a smooth barrier corner at the recess opening, which proves to be beneficial for the subsequent seed layer deposition [10].

In the simulation the bombardment was achieved by increasing the ratio of Argon over barrier metal flux. This could be achieved by increasing the plasma power. In practice it is much easier to control the bombardment by varying the bias power, i.e. by changing the energy of the impinging Argon ions.

Bottomless I-PVD Ta(N) on blanket wafers and single damascene oxide trenches

Two different experimental approaches were tested. In the first, 30 nm Ta(N) barrier layer was deposited and followed by a re-sputter step within the I-PVD chamber. The previously deposited barrier is removed from the recess bottom and the material is re-distributed on the side wall. In the second, the 30 nm thick barrier was deposited in two equal steps and each deposition step was followed by a re-sputter step. In Figure 3 the sheet resistance of Ta(N) is given for the different deposition recipes. Based on these blanket wafer tests recipe I gave rise to 32% (11-12 nm), while recipe II resulted in 50% (15 nm) re-sputtering. The advantage of the first approach is the better uniformity (2.5% vs. 11.4%), while the second concept results in a more effective re-sputtering. As the nitrogen flow is removed during the re-sputter step, the second approach however can give rise to a lower nitrogen content of the film. The nitrogen introduction and the start of the sputtering from the DC-target and RF-coil is simultaneous, because otherwise the coil would be poisoned during a continuous processing. Furthermore, in the case of recipe II more Ar can be incorporated into the film as compared to recipe I, because the physical bombardment of the substrate is increased owing to the two re-sputter steps.

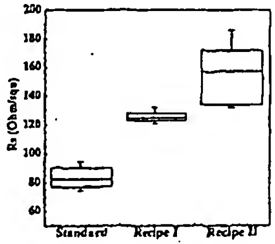

Figure 3 Sheet resistance of the different I-PVD Ta(N) recipes

The bottomless barrier recipes were evaluated by TEM on oxide trenches. The trench depth was 1 µm corresponding approximately to the targeted dual damascene via+metal2 height. Figure 4 compares the bottom coverage for standard and Bottomless I-PVD Ta(N).

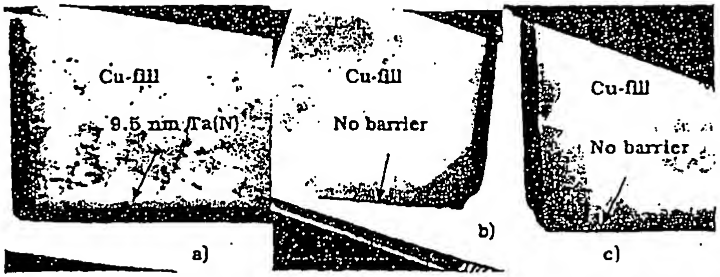

Figure 4 TEM images recorded from the bottom of 1 μm deep 0.25 μm wide trenches. The trenches were filled by ECD copper in order to facilitate the TEM sample preparation.
a) Standard Ta(N) deposition; b) Recipe I for Bottomless I-PVD Ta(N);
c) recipe II for Bottomless I-PVD Ta(N)

The bottom coverage is reduced, while a good sidewall coverage is still maintained due to re-sputtering from the trench bottom. From the TEM image it appears as if a very thin (<2.5 nm) barrier was still present for the bottomless recipes. Note, however, the evolution of the shape of the bottom trench corners. The standard Ta(N) deposition does not change the rounded shape of the bottom corners, as opposed to the bottomless deposition, which gives rise to a step-like corner. The re-sputtering at the bottom is very efficient and after having removed all of the Ta(N) the underlying dielectric is etched. Measuring the Si_3N_4 etch stop layer beneath the trench shows that after punching through Ta(N) recipe I and II reduce the Si_3N_4 thickness by 10 nm and 15 nm, respectively. In the case of a dual damascene architecture the application of the bottomless recipe implies that also some copper from the underlying metal line is re-sputtered. Since the side wall of the recess is covered by the previous barrier deposition and because the adhesion of copper on Ta(N) is good, no performance decrease of the interconnect is expected. On the other hand it is obvious that the duration of the re-sputter step has to be optimized for different geometries (i.e. trench/via depth, design rule, etc.).

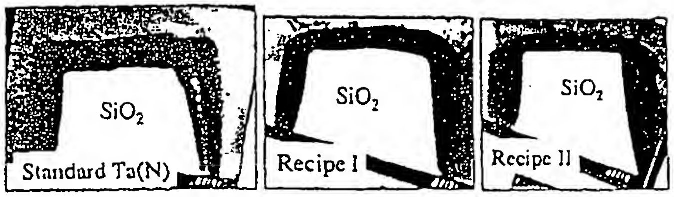

Figure 5 TEM from the top corners of the oxide trenches

In figure 5 the top parts of the trenches are given for the different recipes. Due to the physical bombardment the top corners are rounded and the field coverage is reduced. On the one hand this does not impact on the barrier properties of Ta(N), because the top is removed by CMP. On the other hand the rounded corners result in less overhang by the copper seed-layer deposition [9] and therefore a larger process window for ECD copper filling is given.

In figure 6 the Ta(N) layer thickness is summarized as measured from the TEM pictures at different positions of the trench. The removal of the Ta(N) from the field is approximately as it could be expected from the blanket wafer tests; 10 nm for recipe I and 15 nm for recipe II. The reduction of the Ta(N) thickness on field impacts to some extent on the necessary CMP time to clear the wafers.

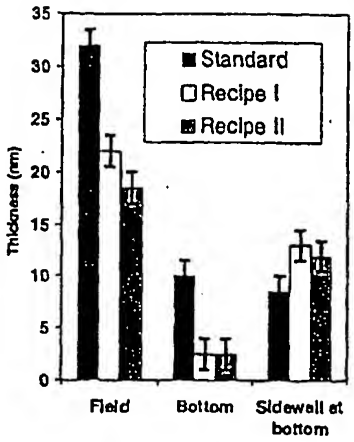

Figure 6 Step coverage for I-PVD Ta(N) with different deposition recipes.

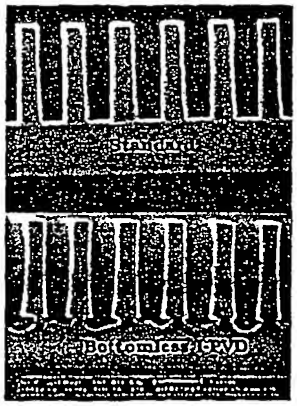

Figure 7 Ta(N) deposited onto 0.25 μm wide trenches. HF invaded through the bottom and etched the oxide to prove absence of the barrier metal at the bottom of patterns.

As compared to the standard recipe the bottom side wall coverage is increased due to the re-sputtering from the bottom. Note also that the side wall coverage at the bottom is similar for recipes I and II. This confirms that both recipes re-sputter completely the barrier from the trench bottom, since upon the increased physical bombardment (recipe II vs. recipe I) no further increase of the side wall coverage is observed.

In order to complement the above data HF-dip tests were performed. The Ta(N) barrier layer was deposited onto oxide trenches and to reveal the weakest points of the Ta(N) barrier coverage, pieces were dipped into 1% HF and inspected by X-SEM. Figure 7 gives the result for 0.25 μm wide trenches. For the Bottomless I-PVD Ta(N) the underlying dielectric is attacked at the bottom of the trenches showing that indeed the bottom barrier layer was extremely thin or not present.

TEM evaluation of via-chains

In a next step the barrier deposition recipes were evaluated on a dual damascene structure. Figure 8 shows the TEM pictures taken from different positions of via chains. In figures 8a-c the cross sections of the full stack are given and good filling of the trench and via holes is observed for all process splits. In figures 8d-f zooms to the metal 2 trench bottoms are provided. The physical sputtering of the wafer results in the reduction of the barrier layer at the metal 2 trench bottom as well. For EM performance and adhesion the presence of a barrier layer at the metal 2 trench bottom is required. With the current recipes this requirement is fulfilled. It is important to note that without the complete clearance of the barrier from the metal 2 trench bottom the barrier thickness on the via bottom converges to zero for recipe II. In the case of the standard barrier deposition the Ta(N) layer is continuous (figure 8g). For recipe I still a continuous barrier is observed on the via hole bottom (figure 8e) even though the thickness is reduced. For recipe II the via bottom is punched through (figure 8f) and discontinuous. The underlying metal 1 copper line was also deepened at places where the barrier layer was completely removed and upon continued barrier resputtering metal 1 copper is deepened. On those places copper is directly plated on the metal 1 copper, which results in copper grains that traverse the original barrier/ metal 1

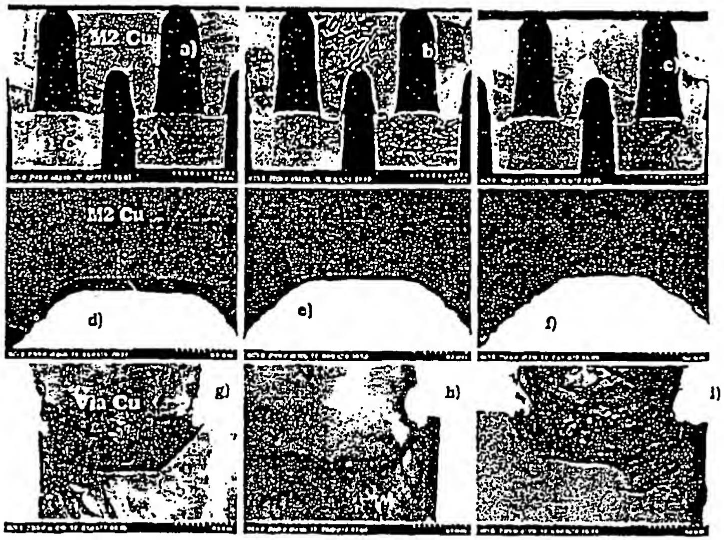

Figure 8 TEM images taken from standard via chain structures with 0.25 μm wide vias. The metal 1 and 2 trenches are 0.35 μm wide.
a-c) full stack; d-f) metal 2 trench bottom; g-i) via bottom

interface.

In figure 9 the Ta(N) thickness values are summarized for the different recipes. As compared to the standard barrier deposition recipe an important decrease of the bottom via coverage is observed. For recipe II the barrier layer is not continuous; the error bar goes below zero. As expected, the via sidewall coverage is increased due to the re-sputtered Ta, while on the metal 2 trench bottom the coverage is decreasing with the increased physical bombardment. This shows on the one hand that a process window exists for the bottomless barrier deposition, but on the other hand it demonstrates also that the re-sputtering recipe has to be fine tuned every time, when the geometry of the dual damascene stack is altered.

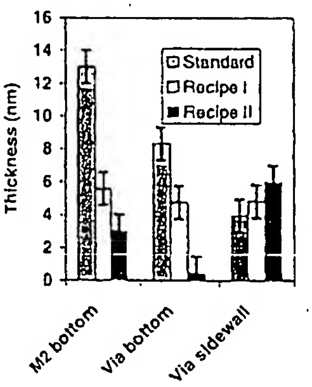

Figure 9 Step coverage on via chain structures.

Via Resistance

The removal of the high resistivity barrier from the via bottom leads to a contact resistance decrease. In figure 10 the single contact resistance is given for the different recipes. Indeed, as compared to the standard barrier, recipe I results in a substantial decrease of the via resistance. This is due to the thinner barrier layer on the via bottom. Recipe II gives also a lower contact resistance than the standard, but higher than recipe I. This is surprising, since in this case the barrier is completely removed from the via bottom. A probable explanation is that it is linked to the worse uniformity of recipe II as contrasted to recipe I.

For via chains (figure 11), also a decrease of the resistance can be observed in the case of the bottomless I-PVD Ta(N) recipes. Note however that in the case of via chains the contribution of the metal 1 and metal 2 resistance to the total resistance is not negligible. For that reason the split up of the data is less important than for the single contacts.

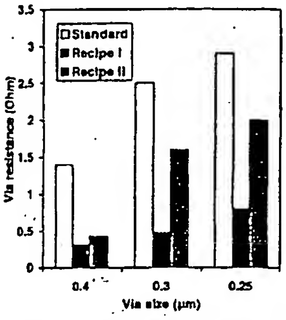

Figure 10 Single contact resistance median valus.

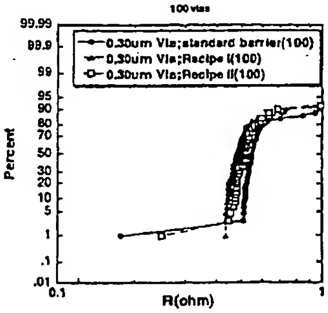

Figure 11 Resistance per one via in a via chain structure

CONCLUSIONS

A new barrier deposition technique was developed called bottomless I-PVD Ta(N) for dual damascene applications. After deposition of the standard I-PVD barrier layer Ta(N) is re-sputtered from the bottom of the vias in the Ta-chamber. The physical sputtering resulted in decreasing the barrier thickness on the metal 2 trench bottom as well. The sidewall coverage is increased due to redeposition. The via resistance is decreased as a result of the thinner or absent high resistivity barrier metal from the via hole bottom.

ACKNOLEDGMENT

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